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(54) CIRCUIT FOR DRIVING AN IMAGE DISPLAY DEVICE.

(57) Circuit for driving an image display device which energizes individual pixels by selecting each of the rows and each of the columns of an active matrix panel (1) in which a plurality of pixels are arranged in the form of a matrix, using clock pulses of predetermined frequency. This circuit is provided with counters (50 and 60) that count clock pulses to issue a binary count value and an inverted output thereof, and decoders (51 and 61) that decode the counter outputs and that generate pulses which shift in synchronism with the clock pulses to each of the rows or columns. With this structure, the switching transistors constituting the decoders (51 and 61) can be switched in a reduced period of time.

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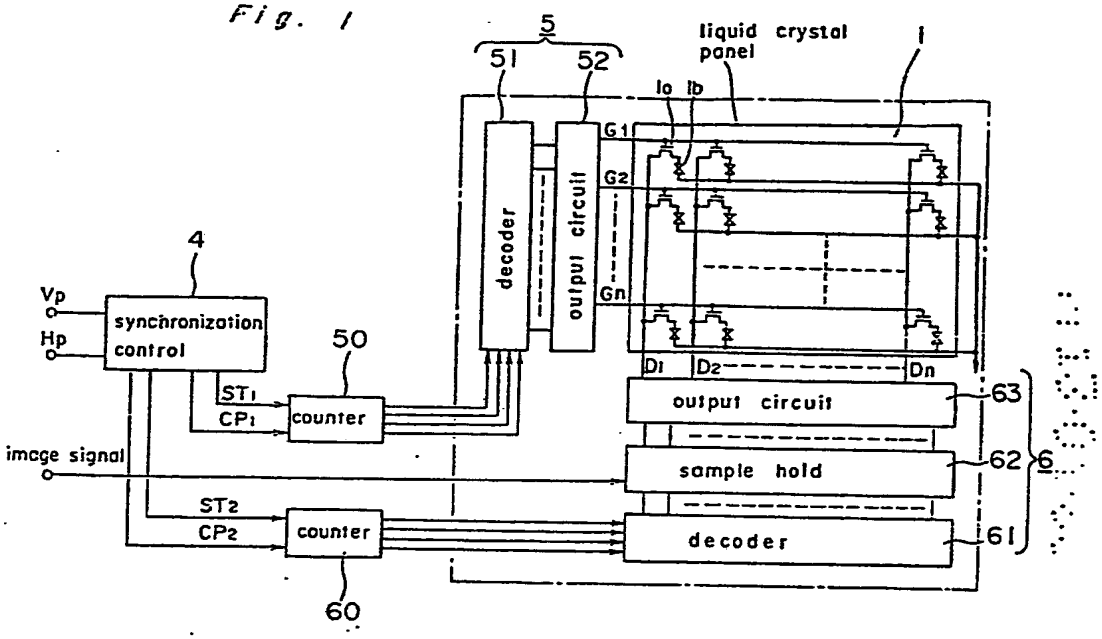
Fig. 1


5
51
52
liquid crystal panel
1
Io
Ib
G1
G2
Gn
decoder
output circuit
4
Vp
Hp
synchronization control
50
ST1
CP1
counter
image signal
ST2
CP2
counter
60
D1
D2
Dn
output circuit
63
sample hold
62
6
decoder
61

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SPECIFICATION

TITLE OF THE INVENTION

A Driving Circuit for an Image Display Apparatus

TECHNICAL FIELD

The present invention relates to a driving circuit for the image display apparatus of liquid-crystal matrix panels.

BACKGROUND OF THE INVENTION

Fig. 18 shows the driving circuit for the liquid-crystal display apparatus by the active matrix liquid-crystal panels to be used in the liquid-crystal TV apparatus. Such a circuit as described hereinabove is described in, for example, Japanese Patent Application Laid-Open Publication Tokkaisho No. 57-41078.

In the same drawing, the liquid-crystal panel 1 of the active matrix type has n column of picture elements in the X direction and m row of picture elements in the Y direction. The TFTs (thin film transistors) 1a composed of m x n amorphous silicone (a-Si) and the liquid-crystal electrodes 1b are connected in matrix shape as shown with the respective rows G1, G2, ... Gm and the respective columns D1, D2, ... Dn being respectively connected with the row driver 2 and the column driver 3. The row driver is composed of the m stage of shift register 2a and output circuit

2b. The column driver is composed of the n stage of shift register 3a, the sampling hold circuit 3b and the output circuit 3c. The synchronization controlling circuit 4 generates the first and second start pulses ST1 and ST2 and the first and second clock pulses CP1 and CP2 in accordance with the horizontal synchronizing signal H_p and the vertical synchronizing signal V_p.

The first start pulse ST1 synchronized with the vertical synchronizing signal and the first clock pulse CP1 synchronized with the horizontal synchronizing signal are fed into the shift register 2a, the voltage waveforms shifted 1H (1 horizontal period) by 1H are applied upon each row G1, G2, ... The TFTs 1a of each line are sequentially turned on in the horizontal retrace section by the voltage waveform to apply the liquid-crystal driving voltage upon each picture element.

On the other hand, the column driver repeats the same operation in each 1H section.

The second start pulse ST2 synchronized with the horizontal synchronizing signal and the second clock pulse of the frequency of the period $\tau=T5/n$ are fed into the shift register 3a, the pulse sequentially shifted τ by τ is outputted to the output of each stage of the shift register 3a. Each stage of the sample holding circuit 3b is controlled by the output of the shift register of each of the corresponding stages, the voltage value of the image signal

is sampled by the falling of the output to hold it till the sampling time (for 1H). The output circuit 3c receives the output of the sampling hold circuit to buffer-amplify to drive the column electrode.

The shift register in the above-described driving circuit is of such construction as shown in Fig. 19. As the transfer of the data, as apparent from Fig. 19 (the drawing shows one stage portion), is performed through the sequential switching operation of four transistors per stage of the shift register by clock ϕ, $\bar{\phi}$, the delay time per stage of transistor is required to be within one fourth of the clock period for the operation. Namely, as the comparatively fast switching speed is required for the transistor, the transistor of the slow switching speed like the a-Si TFT in use for the liquid-crystal panel 1 can not be used.

OBJECTS OF THE INVENTION

Accordingly, an object of the present invention is to provide a transistor of comparatively slow switching speed in one portion of the driving circuit.

Another object of the present invention is to reduce the consumption power of the driving circuit.

A further object of the present invention is to provide a driving circuit where large transient current does not flow to the output circuit when the output signal is switched, and the switching time does not become long.

A still further object of the present invention is to properly operate the panel and to improve the yield even if something goes wrong with the matrix panel or the driving circuit.

SUMMARY OF THE INVENTION

The present invention provides a driving circuit for the image display apparatus, wherein the respective rows and columns of the active matrix panel with a plurality of picture elements being disposed in the matrix shape are respectively selected by the clock pulses of the given frequency to drive each of the picture elements. The present invention is characterized in that a counter for counting the clock pulses to introduce the binary count values and their inversion outputs, and a decoder for decoding the counter outputs to generate pulses, which sequentially shift in synchronous relation with the clock pulses, into the respective rows or the respective columns are provided, the switching transistor constituting the decoder is formed as a thin film transistor on the same base plate as the active matrix panel. Accordingly, the driving circuit is composed of a counter which is adapted to count the clock pulses to introduce the binary count values and their inversion outputs, a decoder which is adapted to generate the pulses that sequentially shift in synchronous relation with the clock pulses into the respective rows and/or the respective columns of the matrix panel, so that

the time required for the switching operation of the switching transistor within the driving circuit is adapted to become shorter by the above-described means.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and features of the present invention will become apparent from the following description taken in conjunction with the preferred embodiments thereof with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram showing a driving circuit for a liquid-crystal display apparatus by the active matrix liquid crystal panel to be used in th liquid crystal as a first embodiment of the present invention;

Fig. 2 is a circuit diagram showing the concrete construction of the first decoder of Fig. 1;

Fig. 3 is a circuit diagram showing the concrete construction of the output circuit of Fig. 2;

Fig. 4, Fig. 5 and Fig. 6 are, respectively, circuit diagrams each showing a modification of the output circuit of Fig. 3;

Fig. 7 and Fig. 8 are, respectively, circuit diagrams each showing a modification of the row driver of Fig. 1;

Fig. 9 and Fig. 10 are, respectively, circuit diagrams each showing the concrete construction of the row driver of Fig. 1;

Fig. 11 is a block diagram showing a driving circuit for the liquid-crystal display apparatus as a second embodiment of the present invention;

Fig. 12 is a circuit diagram showing the concrete construction of the first decoder of Fig. 11;

Fig. 13 is a block diagram showing a driving circuit for the image displaying apparatus as a third embodiment of the present invention;

Fig. 14 is a block diagram showing a modification of Fig. 13;

Figs. 15(a) through 15(f) are illustrating drawings showing the processes for forming on the same base plate the p channel TFTs and the n channel TFTs in the circuit of Fig. 13;

Figs. 16(a) through 16(c) are waveform charts in each portion of the row driver of Fig. 1;

Figs. 17(a) through 17(c) are waveform charts in each portion of the column driver of Fig. 1;

Fig. 18 is a block diagram showing the driving circuit of the conventional liquid-crystal display apparatus; and

Fig. 19 is a circuit diagram showing the concrete construction of the shift register of Fig. 18.

DETAILED DESCRIPTION OF THE INVENTION

Before the description of the present invention proceeds, it is to be noted that like parts are designated

by like reference numerals throughout the accompanying drawings.

(First Embodiment)

Referring to the drawings, there is shown in Fig. 1 a block diagram showing a driving circuit for a liquid-crystal display apparatus with active matrix liquid-crystal panel to be used in a liquid-crystal TV apparatus according to a first preferred embodiment of the present invention, which includes a liquid-crystal panel 1, output circuits 52, 63, a sample holding circuit 62, decoders 51, 61, a synchronization controlling circuit 4, and counters 50, 60.

The active matrix type of liquid-crystal panel 1 has picture elements of n column in the X direction, m row in the Y direction, a TFT (thin film transistor) 1a and a liquid-crystal electrode 1b composed of an amorphous silicon (a-Si) of m x n connected into a matrix shape as shown, the respective rows G1, G2, ... Gm and the respective columns D1, D2, ... Dn are respectively connected with row driver 5 and a column driver 6. The row driver 5 is composed of a decoder 51 and an output circuit 52, the column driver 6 is composed of a decoder 61, a sample holding circuit 62 and an output circuit 63. The synchronization controlling circuit 4 generates the first and second start pulses ST1 and ST2 and the first and second clock pulses CP1 and CP2 in accordance with horizontal synchronizing signals H_p and vertical synchronizing signals V_p.

Fig. 16 shows each waveform of the row driver 5, reference character a shows a picture signal with a vertical synchronizing signal V_p and a horizontal synchronizing signal H_p being placed one upon another. In the drawing, reference character T1 shows the vertical synchronizing signal section, reference character T2 shows the vertical retrace section, and reference character T3 is the picture signal section.

On the other hand, each portion waveform of the driver 6 is shown in Fig. 17. The column driver repeats the same operation in each 1H section. Fig. 17(a) is a picture signal wherein 1H section in T3 is expanded and drawn. In the drawing, reference character T4 shows a horizontal retrace section and reference character T5 shows the picture information-contained section.

The second start pulses ST2 synchronized with the horizontal synchronous signal shown in Figs. 17(b) and 17(c), and the second clock pulses of the frequency of the period $\tau=T5/n$ are fed to the counters 50 and 60.

The counter 50, which is the first counter, starts the counting operation of the first clock pulses CP1 with the first start pulse ST1 from the synchronization controlling circuit 4 to output the binary count outputs A and B and to output the inversion outputs $\bar{A}$ and $\bar{B}$. This counter is composed of IC:LC4520B and LC4049B manufactured by Tokyo Sanyo Electric Co., Ltd. The decoder 51 is the first

decoder, which decodes the first counter output to respectively output the pulses that become high sequentially for each of the first clock pulses CP1 to the right and left of each row G1, G2, ... The counter 60 is the second counter, which is adapted to output the binary outputs in accordance with the second start pulse ST2 and the second clock pulse CP2 from the synchronization controlling circuit 4. The decoder 61 is the second decoder, which decodes the second counter output to output the pulses that become high sequentially for each of the second clock pulses CP2 to each column D1, D2, ... The row driver 5 is composed of the first counter 50, the first decoder 51 and the output circuit 52. The column driver 6 is composed of the second counter 60, the second decoder 61, the sample holding circuit 62 and the output circuit 63. And the first and second decoders 51 and 61, the output circuits 52 and 63, and the sample holding circuit 62 are formed of the a-Si TFT in the same process and on the same base plate as on the liquid-crystal panel 1.

The concrete circuit of the first decoder and the operation of the row driver will be described with reference to Fig. 2. Each row of the binary count outputs A and B from the first counter 50 and the inversion outputs $\bar{A}$ and $\bar{B}$, and each row G1, G2, ... are crossed in the matrix shape with two TFTs composing an AND gate being disposed in series in each row. In addition, each row has loads TFT T9 through

T12 connected therewith. The output circuit 52, which has such construction as shown in Fig. 3, is connected with the outputs for each of the rows.

Now, when the counter output is "00", A and B are both "0", $\bar{A}$ and $\bar{B}$ are both "1" to turn on the TFTs T1, T2, T4 and T5, with only the row G1 becoming high. Then, when the counter output is "01", both A and $\bar{B}$ are "0", both $\bar{A}$ and B are "1" to turn on the TFTs T2, T3, T4 and T7, with the row G2 becoming high. Upon sequential increment of the counter output like this, the next row becomes sequentially high so as to be selected and to be amplified in reversion in the output circuit of the next stage, and thus the TFTs within the liquid-crystal panel of this row.

When the driving operation of all the rows is completed, and the first counter 50 is reset by the next start signal, the scanning operation of the next frame is started.

Fig. 4 shows a circuit diagram of one row portion of the output circuit in the present embodiment. A first FET T17 for amplification and a second FET T18 for loading are longitudinally connected between the power supply V_{DD} and an earth, the gate of the second FET T18 being connected with the power supply V_{DD}. And the input signal is applied upon the gate of the first FET T17 so that the output signal is outputted from the connection point between the first and second FETs T17 and T18. With the circuit of Fig. 4, when

the input signal is high, the first and second FETs T17 and T18 are turned on, thus the output becomes high. At this time, the current does flow to the output gate circuit constituted by the first and second FETs T17 and T18.

On the other hand, when the input signal is low, the first and second FETs T17 and T18 are turned off, thus resulting in the low output. At this time, the current does not flow into the output gate of the first first and second FETs.

Accordingly, in the present embodiment, the current flows to the output circuit of one row portion selected from among two hundred forty rows, but the current does not flow at all to the output circuit of the other two hundred thirty-nine rows.

Also, Fig. 5 shows the other embodiment of the output circuit, wherein the third and fourth FETs T19 and T20 for load use and amplification use are connected in the same manner as in Fig. 4 to provide the two-stage construction.

In the above-described embodiments, the present invention is applied only upon the row driver. Needless to say, it may even be applied the column driver.

Fig. 6 shows a circuit diagram of one row portion of the output circuit in the present embodiment. The first and second FETs T17 and T18 for amplification are longitudinally connected between the power supply V_{DD} and an earth.

And the input signal is applied upon the gate of the first FET T17 so that the output signal is outputted from the connection point between the first and second FETs T17 and T18. The reversion output which has been reversed by the inverter composed of the third and fourth FETs T19 and T20 is applied upon the gate of the second FET T18.

The operation will be described hereinafter. When the input signal is high, the first FET T17 is turned on. The fourth FET T20 also becomes high at the gate to turn on the fourth FET so as to turn off the second FET T18. Thus, the output becomes high. At this time, the comparatively small current flows to the third and fourth FETs T19 and T20 which constitute the inverter, but the current does not flow to the output gate circuit constituted by the first and second FETs T17 and T18.

On the other hand, when the input signal is low, the first FET T17 is turned off and the second FET T18 is turned on, thus resulting in the low output. In the above case, the current does not flow into both the inverter and the output gate.

Namely, the current does not flow in the steady-state condition with the small amount of current flowing the first first and second FETs at the switching operation.

Accordingly, in the present embodiment, the current flows to the output circuit of one row portion selected from among two hundred forty rows, but the current

does not flow at all to the output circuit of the other two hundred thirty-nine rows.

According to the embodiments, the power consumption in the driving circuit may be considerably reduced so as to make the image display apparatus for the liquid-crystal TV or the like smaller in size.

Fig. 7 shows the other embodiment of the first decoder. The first decoder 51' of the present embodiment is a NAND gate, wherein the TFTs T1 through T8 are disposed parallel to each row, with the advantage that the driving voltage may be made lower through the power consumption and the wiring number are a little more than in Fig. 2.

Furthermore, the other embodiment of the first decoder is shown in Fig. 8. The first decoder 51' of the present embodiment is an AND gate, where the diodes D1 through D8 are disposed parallel to each row, with the advantage that the driving voltage is lower and the number of the wirings is fewer though the power consumption is large.

In Fig. 2, Fig. 7 and Fig. 8, the first decoder actually needs about 240 in the row number to increase the column number of the counters though the first decoder shows only four-row portion for simplification. Also, as the second counter 60 and the second decoder 61 in the column driver 6 are fundamentally similar in construction and operation to those of the row driver 5, they are not shown.

According to the embodiments as described hereinabove, one portion of the driving circuit may be construction on the same base plate as the switching transistor located within the active matrix panel and with the switching transistor of the same construction through the same process, so that the external circuit of the matrix panel may be considerably simplified and the connection wires between the matrix panel and the external circuit may be considerably reduced in number.

The other embodiment will be shown in Fig. 9 as the concrete circuit of the row driver. Each code signal line of the binary count outputs A, B and inversion outputs $\bar{A}$, $\bar{B}$ from the first counter 50 is crossed in the matrix shape with respect to the lines L1 through L4 provided corresponding to each row G1, G2 of the matrix panel. The TFTs T1 through T8 constituting two AND gates are arranged for each row, so that the high is adapted to be outputted into each of the lines L1 through L4 when either of the respective rows G1, G2, ... is selected.

Also, each of the code signal lines is crossed in the matrix shape with respect to the adjacently disposed lines L1' and L4' in addition to the lines L1 through L4 corresponding to each row G1, G4, ... The TFTs T1' through T8' are arranged similarly on each line, so that the low is adapted to be outputted upon each line L1' through L4' when either of the respective rows G1, G2, ... is

selected. Namely, the output of the opposite phase appears on the adjacent two lines L1 and L1'.

The output circuit 52 is composed of a pair of longitudinally connected first and second FETs T17 and T18 for each row G1, G2, ..., with each row G1, G2, ... being connected from the connection point between both the FETs. And the lines L1 through L4 are combined with each gate of the first FET T17, the lines L1' through L4' are combined with each gate of the second FET T18.

The operation will be described hereinafter. Now, when the counter output is "00", both the A and B become "0", both the $\bar{A}$ and $\bar{B}$ become "1" to turn on the TFTs T1, T2, T4 and T5 and T1', T2', T4' and T5', so that the line L1 becomes high, the lines L2 through L4 become low, furthermore, the line L1 becomes low, the lines L2' through L4' become high. Accordingly, the first FET T17 turns on, the second FET T18 turns off to output the high output into the row G1. At this time, the first FETs of the other lines are all off, the second FETs thereof are all on with all the outputs being low.

Then, when the counter output is "01", the A, $\bar{B}$ become "0", the $\bar{A}$, B become "1" to turn on the TFTs T2, T3, T4 and T7 and T2', T3', T4' and T7', so that the line L2 becomes high, the lines L1, L3 and L4 are low, furthermore the line L2' becomes low, the lines L1', L3' and L4' become high. Thus, the first FET T17 of second row G2 turns on,

the second FET T18 turns off to output the high output to the row G2.

As the counter outputs sequentially increase as described hereinabove, the next row sequentially becomes high and is selected to drive the TFT within the liquid-crystal panel of that row.

And the driving operation of all the rows is completed to reset the first counter 50 by the next start signal, so that the next frame scanning operation is started.

In the above-described row driver, the decoder simultaneously outputs two signals opposite in phase in accordance with each row to apply the completely opposite-phase signals upon each gate of the first and second FETs, so that the current does not flow at all in the steady-state condition. As the switching delay of one FET is not caused, both the FETs simultaneously do not turn on during the switching operation so that the large transient current does not flow. Fig. 10 shows the other embodiment of the row driver. In this embodiment, the first and second FETs T17 and T18 of the decoder 51 and the output circuit 52 are respectively divided and disposed on both the sides of the liquid-crystal panel 1 and may be symmetrically arranged at right and left.

It is to be noted that the operation is completely the same as in Fig. 9.

The above-described two embodiments were the description in the row driver. It is clear that the present invention may be applied similarly even to the row driver.

According to the above-described embodiment, the current does not flow at all under the steady condition in the output circuit and the large transient current does not flow even during the switching operation, so that the power consumption of the driving circuit may be reduced. Also, the switching time does not become longer than necessary.

(Second Embodiment)

Fig. 11 is a block diagram showing the driving circuit of the liquid-crystal display apparatus in the other second embodiment. The same reference characters are given to the same portions as in Fig. 1 with the description being omitted.

Referring to Fig. 11, a first counter 50 starts the counting operation of the first clock pulse CP1 by the first start pulse ST1 from the synchronization controlling circuit 4 to output the binary count outputs A, B and the inversion outputs $\bar{A}$, $\bar{B}$. The first decoders 51, 51 decode the first counter outputs to respectively output the pulses, which sequentially become high for each of the first clock pulses CP1 to the right and left of each row G1, G2, ... A second counter 60 outputs the binary counter outputs in accordance with the second start pulse ST2 and the second clock pulse CP2 from the synchronization controlling circuit

4. The second decoders 61, 61 respectively output the pulses, which sequentially become high for each of the second clock pulses CP2 upwardly and downwardly of each column D1, D2, ... through the decoding operation of this second counter output. Thus, the row driver 5 is composed of the first counter 50, the first decoder 51 and the output circuit 52. The column driver 6 is composed of the second counter 60, the second decoder 61, the sample holding circuit 62 and the output circuit 63. And the first and second decoders 51 and 61, the output circuits 52 and 63, and the sample holding circuit 62 are formed on the same base plate as the liquid-crystal panel 1 and through the same process by the a-Si TFT.

The concrete circuit of the first decoder and the operation of the line driver will be described in Fig. 12. The respective rows of the binary count outputs A, B and these inversion outputs $\bar{A}$, $\bar{B}$ from the first counter 50 are crossed in the matrix shape with respect to the respective rows G1, G2, ..., with two TFTs constituting the AND gate being disposed in series on the respective rows. In addition, the loads TFTs T9 through T12 are connected with the respective rows with the output circuit 52 being connected with the output for each of the rows.

Now, when the counter output is "00", both the A, B are "0", both the $\bar{A}$, $\bar{B}$ become "1" to turn on the TFTs T1, T2, T4 and T5, so that only the row G1 becomes low. Then,

when the counter output is "01", both the A, $\bar{B}$ are "0" and both the $\bar{A}$, B become "1" to turn on the TFTs T2, T4, T7, so that the row G2 becomes low. As the counter output sequentially increases like this, the next row sequentially becomes low so as to be selected and is amplified in inversion by the output circuit of the next stage, so that the TFT within the liquid-crystal panel of this row is driven.

And when the driving operation of all the rows is completed to reset the first counter 50 by the next start signal, the scanning operation of the next frame is started.

Although the decoder 51 and the output circuit 52 are shown only in the left-hand side portion of Fig. 12, they are really arranged symmetrically in right and left as shown in Fig. 1, with one row being driven by the same signal from the right and left.

Accordingly, even if the scanning line of the liquid-crystal panel 1 is disconnected somewhere at one location, the signals are fed into the entire rows, because the signals are fed from both the sides of the rows, so that the displaying operation is completely performed. Also, when the scanning line and the signal have been short-circuited somewhere in the active matrix, the line defects may be changed into the point defects because of the cutting operation of that portion at two locations, the signal line is crossed on the scanning line.

A case where the fault has occurred on the side of the decoder will be described hereinafter. First, where the short-circuit has been caused between the code signal line from the counter and the line of the AND gate of the decoder, the fault is not caused because of the supply of the output from the other decoder if the line wiring of the AND gate is cut on both the lines of the code signal. Also, even if the line of the AND gate is disconnected somewhere, the compensation may be performed by the output of the other decoder in the same manner as described hereinabove.

Furthermore, if the disconnection is caused on the code signal line of the decoder, the operation is not interfered with, because the code signals are fed from above and below the matrix.

In addition, when the disconnection has been caused at two locations on the code signal line, the fault line becomes open if the output line of the output circuit corresponding to the gate line existing between the two lines is cut with laser or the like, so that the driving operation may be effected with the signal from the other decoder.

It is clear that the method of applying the code signal from above and below the matrix of the decoder as described hereinabove may be similarly applied to the decoder 61 of the column driver.

According to the embodiment, the operation may be effected without hindrance if the failures such as disconnection, short-circuit or the like occur on the matrix panel or within the driving circuit during the manufacturing process, so that the yield may be considerably improved as compared with the conventional one with the shift register being used in the driving circuit.

The third embodiment wherein the driving circuit of the picture display apparatus of the present invention is shown in Fig. 13 and Fig. 14. Referring to Fig. 13, the first bit a of the binary count is connected with each gate of the p type TFTs 11 and 31 of the first and third row signal lines, of the n type TFTs 21 and 41 of the second and fourth row signal lines, the second bit b is connected with each gate of the p type TFTs 12 and 22 of the first and second row signal lines, of the n type TFTs 32 and 42 of the third and fourth row signal lines.

The counter 50 is composed of two-bit four-output construction. If the true values have been set that the outputs are a="0", b="0" when the counter is 0, the outputs are a="1", b="0" when the counter is 1, the outputs are a="0", b="1" when the counter is 2, the outputs are a="1", b="1" when the counter is 3, the negative voltage signal corresponding to the "0" turns on the p channel TFT, the positive voltage signal corresponding to the "1" turns off the n channel TFT in the decoder 51. Accordingly, as the

TFTs 11, 12, 22 and 31 turn on, the TFTs 21, 32, 41 and 42 turn off when the counter is 0, only the first output signal g1, with the TFTs 11 and 12 of ON condition being operated, among four outputs g1 through g4 from the decoder 51 becomes high. Accordingly, as the TFT 14 turns on in the output circuit 52 composed of n channel TFTs 14, 15, 24, 25, 34, 35, 44 and 45, only the first gate G1 among four gate signals G1 through G4 becomes high.

Then, when the counter 50 advances from 0 to 1, the TFTs 12, 21, 22 and 41 of the decoder 51 turn on, the TFTs 11, 31, 32 and 42 turn off to make the output signal g2 only high, so that only the gate signal G2 becomes high.

As the counter 50 advances like this, the gate signals G1 through G4 sequentially become high to drive the liquid-crystal panel.

Also, in the embodiment of Fig. 14, the output circuit 52' is different from that of the embodiment of Fig. 12. Namely, the circuit 52' complementarily connects the p channel TFTs 14, 24, 34 and 44 with the n channel TFTs 15, 25, 35 and 45. As the TFTs of the p channel TFTs or the n channel TFTs are off with the exception of the switching operation time, the current consumption is smaller.

The process of forming the p channel TFTs and the n channel TFTs on the same base plate, i.e., the active matrix panel, is shown in Fig. 15. As shown in Fig. 15(a), the conductive layer 100 composed of ITO or gold which

becomes the source of the TFT and the drain electrode is attached on the glass base plate s of the active matrix panel to perform the patterning operation on the given pattern with photo-lithography. As shown in Fig. 15(b), the n type of amorphous silicones which become the source, drain electrodes 200, 200 of the n channel TFTs are attached to perform the patterning operation. The p type of amorphous silicones which becomes the source, drain electrodes 300, 300 of the p channel TFTs are attached on them to perform the patterning operation as shown in Fig. 15(c), the former n type of amorphous silicones 200, 200 may remain.

Furthermore, as shown in Fig. 15(d), the i type (genuine) amorphous silicones which become the operation regions 400 of both the TFTs are attached to perform the patterning operation. As shown in Fig. 15(e), insulating film such as SiO_2, Si_3N or the like which becomes the gate insulating film 5 is attached thereon. Finally, as shown in Fig. 15(f), a conductive layer such as aluminum which becomes a gate electrode 600 is attached to perform the patterning operation.

In the above description, the present invention is embodied about the driving circuit on the side of the gate signal line. Needless to say, it may be adopted on the driving circuit on the side of the drain signal line.

According to the picture display apparatus of the present embodiment, the decoder is composed of the combination circuit between the p channel thin film transistor and

the n channel thin film transistor so that the decoding operation may be performed by the use of the binary count value from the counter without the use of the inversion output. Thus, the input lines from the counter into the decoder are halved in number to simplify the construction of the decoder and to improve the yield.

Although the present invention has been fully described by way of example with reference to the accompanying drawings, it is to be noted here that various changes and modifications will be apparent to those skilled in the art. Therefore, unless otherwise such changes and modifications depart from the scope of the present invention, they should be construed as being included therein.

List of Reference Numerals Used in the Drawings

1 ... liquid-crystal panel

4 ... synchronization controlling circuit

50, 60 ... counter

51 ... decoder

52 ... output circuit

63 ... output circuit

62 ... sample holding circuit

61 ... decoder

T ... transistor

D ... diode

What is claimed is:

1. In a driving circuit for an image display apparatus wherein the respective rows and columns of an active matrix panel with a plurality of picture elements being disposed in matrix shape are respectively selected by the clock pulses of the given frequency to drive the respective picture elements, the improvement thereof comprising a counter for counting said clock pulses to introduce binary count values, and a decoder for decoding the counter outputs to generate pulses, which sequentially shift in synchronous relation with said clock pulses, in the respective rows and/or the respective columns.

2. The driving circuit for an image display apparatus in accordance with Claim 1, wherein a switching transistor constituting said decoder is formed as a thin film transistor on the same base plate as said active matrix panel.

3. The driving circuit for an image display apparatus in accordance with Claim 2, wherein said switching transistor is formed by the same process in said active matrix panel.

4. A driving circuit for an image display apparatus comprising a circuit for generating the pulses which sequentially shift in synchronous relation with said clock pulses so as to sequentially select at the period of the clock pulse of the given frequency respectively each row

and/or each column of the panel with a plurality of picture elements being disposed in the matrix shape, and an output circuit for amplifying the pulses to output to said panel, said output circuit including an FET for amplification use having a first electrode to which said pulses are inputted, a second electrode to which the power-supply terminal is connected, a third electrode for outputting the output signals, and a load circuit connected between said third electrode and the earth so that the current flows to said output circuit when said output signal is high in level, the current does not flow to said output circuit when said output signal is low in level.

5. A driving circuit for an image display apparatus comprising a circuit for generating the pulses which sequentially shift in synchronous relation with said clock pulses so as to sequentially select at the period of the clock pulse of the given frequency respectively each row and/or each column of the panel with a plurality of picture elements being disposed in the matrix shape, and an output circuit for amplifying the pulses to output to said panel, said output circuit including a first FET in which said pulses are inputted to the gate, and a second FET connected in cascade with the first FET and in which the signals opposite in phase to said pulses are adapted to be inputted to the gate, so that the output signal is outputted from the connection point of both the FETs.

6. In a driving circuit for an image display apparatus wherein the respective rows and columns of the active matrix panel with a plurality of picture elements being disposed in the matrix shape are respectively selected by the clock pulse of the given frequency to drive each of said picture elements, the improvement thereof comprising a counter for counting said clock pulses to introduce binary count values and their inversion outputs, a decoder for decoding the counter outputs to simultaneously generate a pair of pulses opposite in polarity which sequentially shift in synchronous relation to said clock pulses in each of said respective rows and/or respective columns, and an output circuit including first and second FETs being connected in cascade with a pair of pulses opposite in polarity being applied respectively upon each gate, the output signals amplified from the connection points of both the FETs being adapted to be outputted upon said active panel.

7. In a driving circuit for an image display apparatus wherein the respective rows and columns of an active matrix panel with a plurality of picture elements being disposed in matrix shape are respectively selected by the clock pulses of the given frequency to drive the respective picture elements, the improvement thereof comprising a counter for counting said clock pulses to introduce binary count values and their inversion outputs, and a pair of decoders are respectively connected with both

the ends of each of the rows and/or each of the columns, decode the counter outputs to generate the pulses, which sequentially shift in synchronous relation with said clock pulses, in each of said rows and/or in each of said columns.

8. In a driving circuit for an image display apparatus wherein the respective rows and columns of an active matrix panel with a plurality of picture elements being disposed in matrix shape are respectively selected by the clock pulses of the given frequency to drive the respective picture elements, the improvement thereof comprising a counter for counting said clock pulses to introduce binary count values and their inversion outputs, and a decoder for decoding the counter outputs to generate pulses which sequentially shift in synchronous relation with said clock pulses to each of said rows or each of said columns so as to feed said counter output from both the ends of the code signal line of said decoder.

9. In an image display apparatus wherein the respective rows and columns of an active matrix panel with a plurality of picture elements being disposed in matrix shape are respectively selected by the clock pulses of the given frequency to drive each of said picture elements, the improvement thereof comprising a counter which counts said clock pulses to introduce the binary count values, and a decoder which decodes the counter outputs to generate the pulses for sequentially shifting in synchronous relation

with said clock pulses in each of said rows and/or each of said columns, both of the counter and decoder being disposed in parallel on said active matrix panel, said decoder being composed of the p channel thin film transistor and the n channel thin film transistor, which responds to the binary count value of the counter.

10. The image display apparatus in accordance with Claim 9, wherein the output circuit of the decoder is composed of the p channel thin film transistor and the n channel thin film transistor.

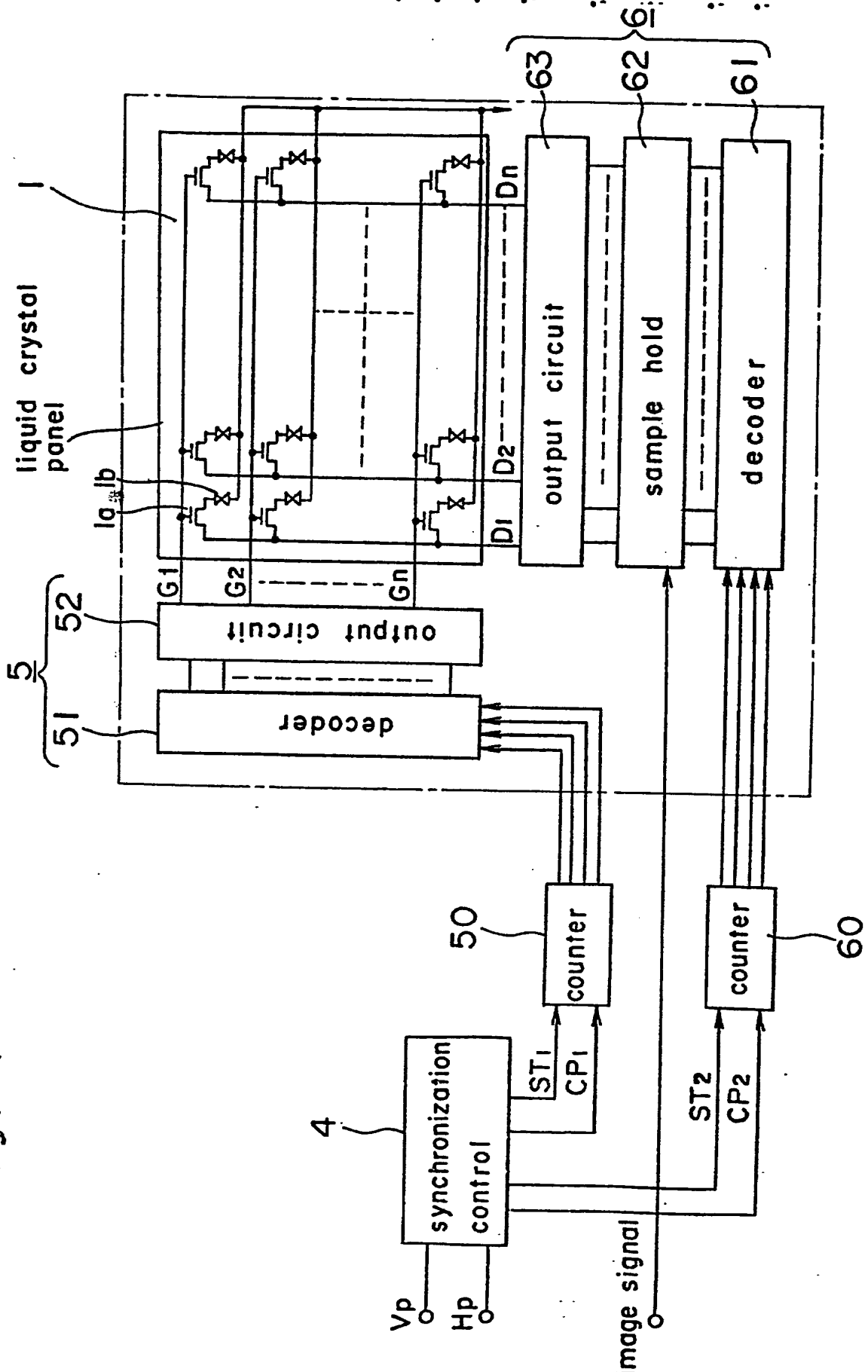

liquid crystal panel
1
Ia
Ib
G1
G2
Gn
D1
D2
Dn
output circuit
sample hold
decoder
61
62
63
6
5
51
52
decoder
output circuit
50
counter
60
counter
4
synchronization control
ST1
CP1
ST2
CP2
Vp
Hp
image signal

Fig. 1

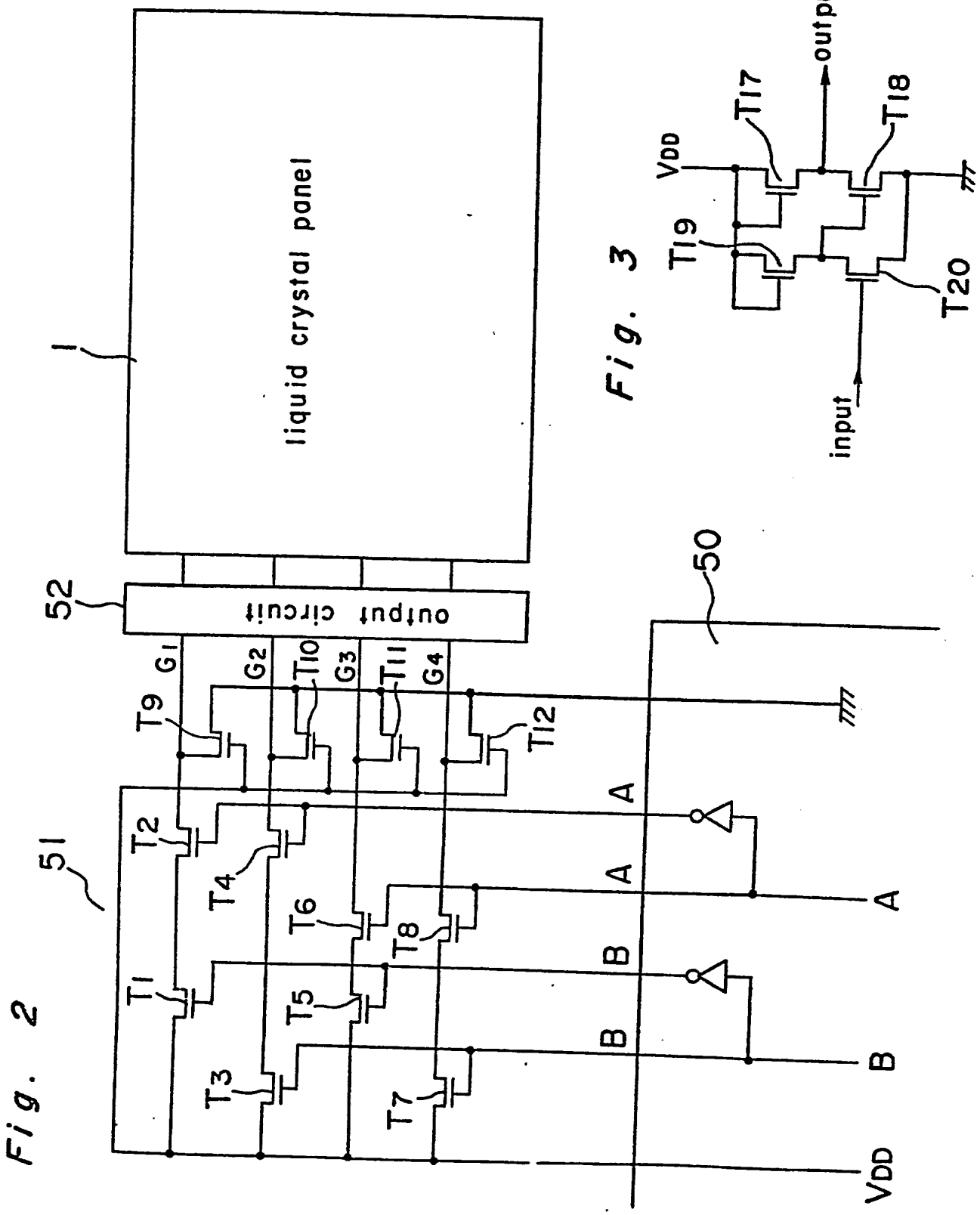

liquid crystal panel
1
output circuit
52
50
51
G1
G2
G3
G4
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
A
A
B
B
VDD

Fig. 2

VDD
T17
output
T18
T19
T20
input

Fig. 3

Fig. 4

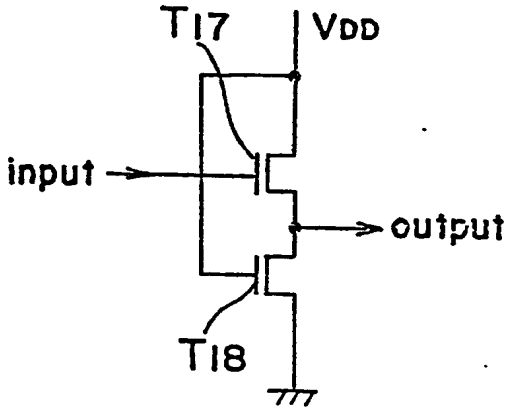


Fig. 5

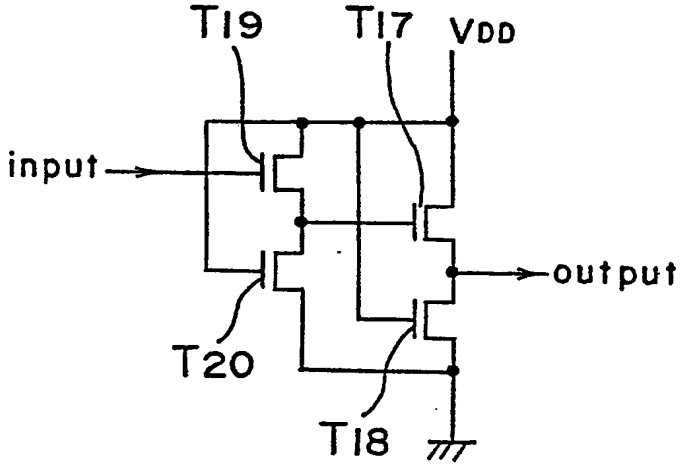
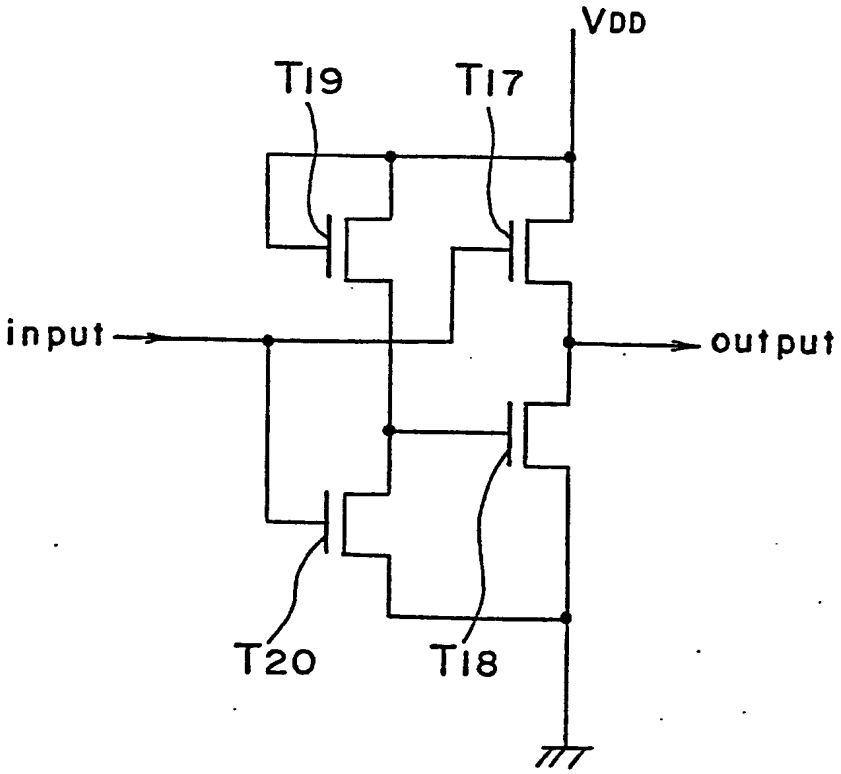


Fig. 6



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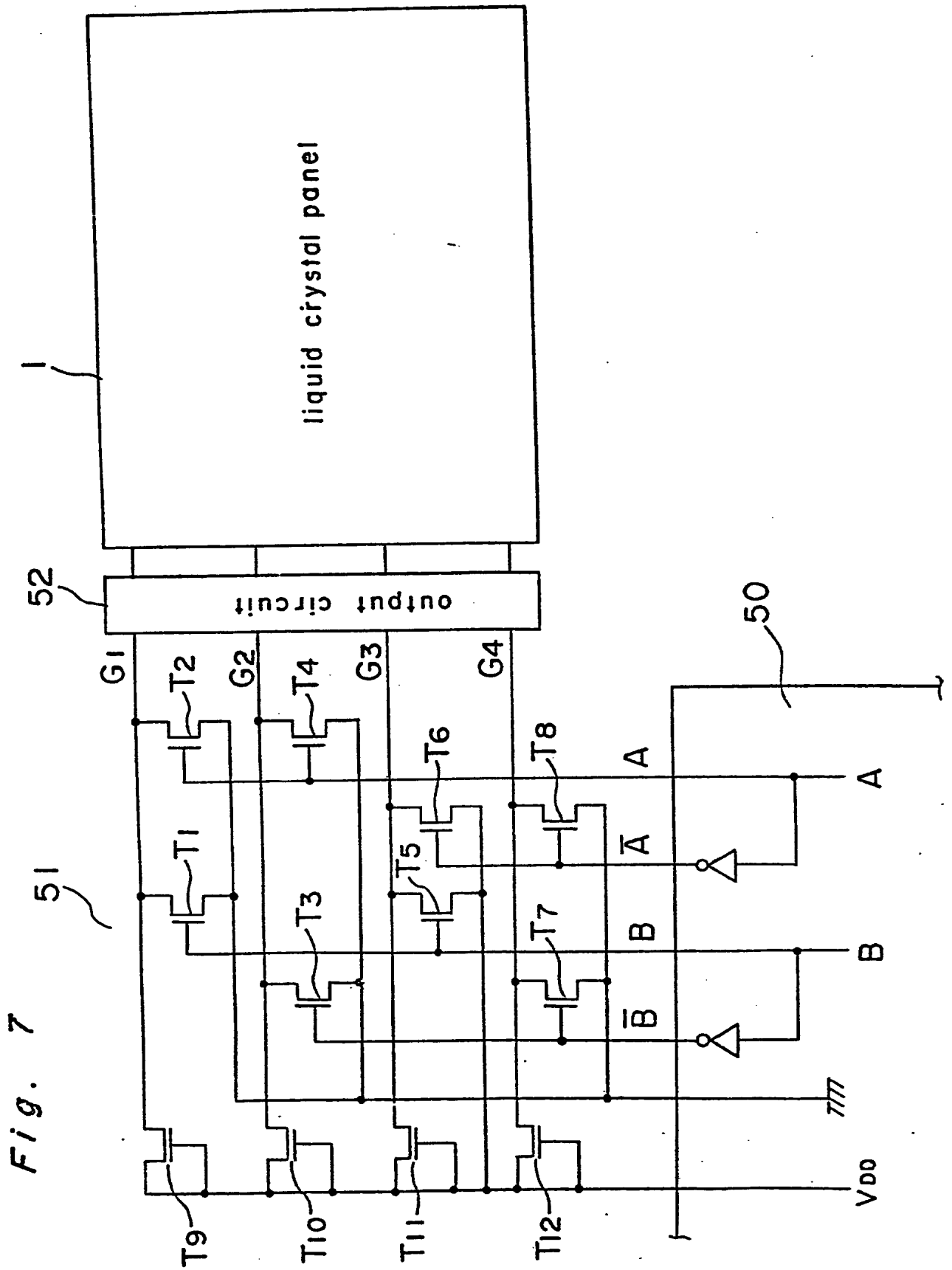


Fig. 7

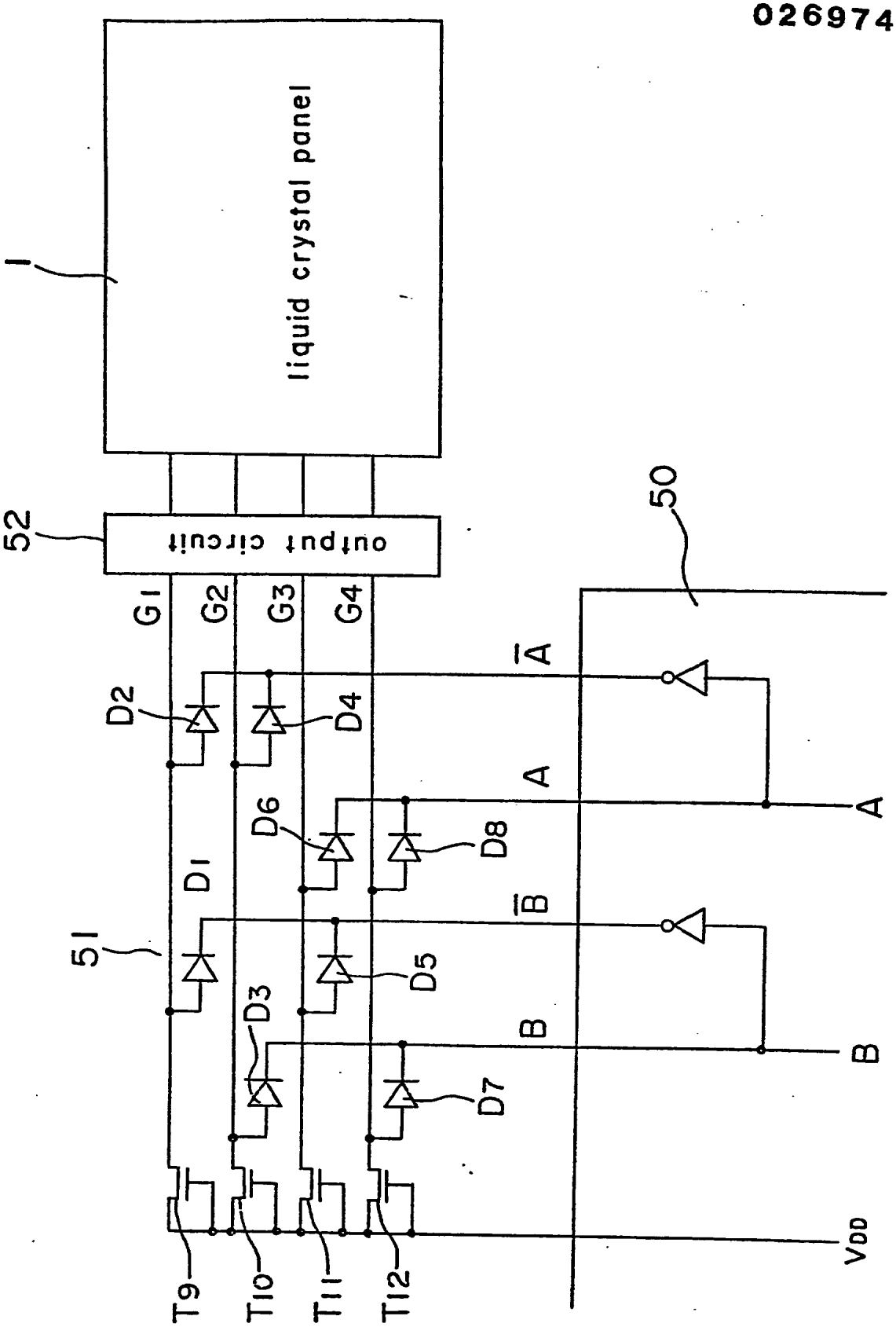
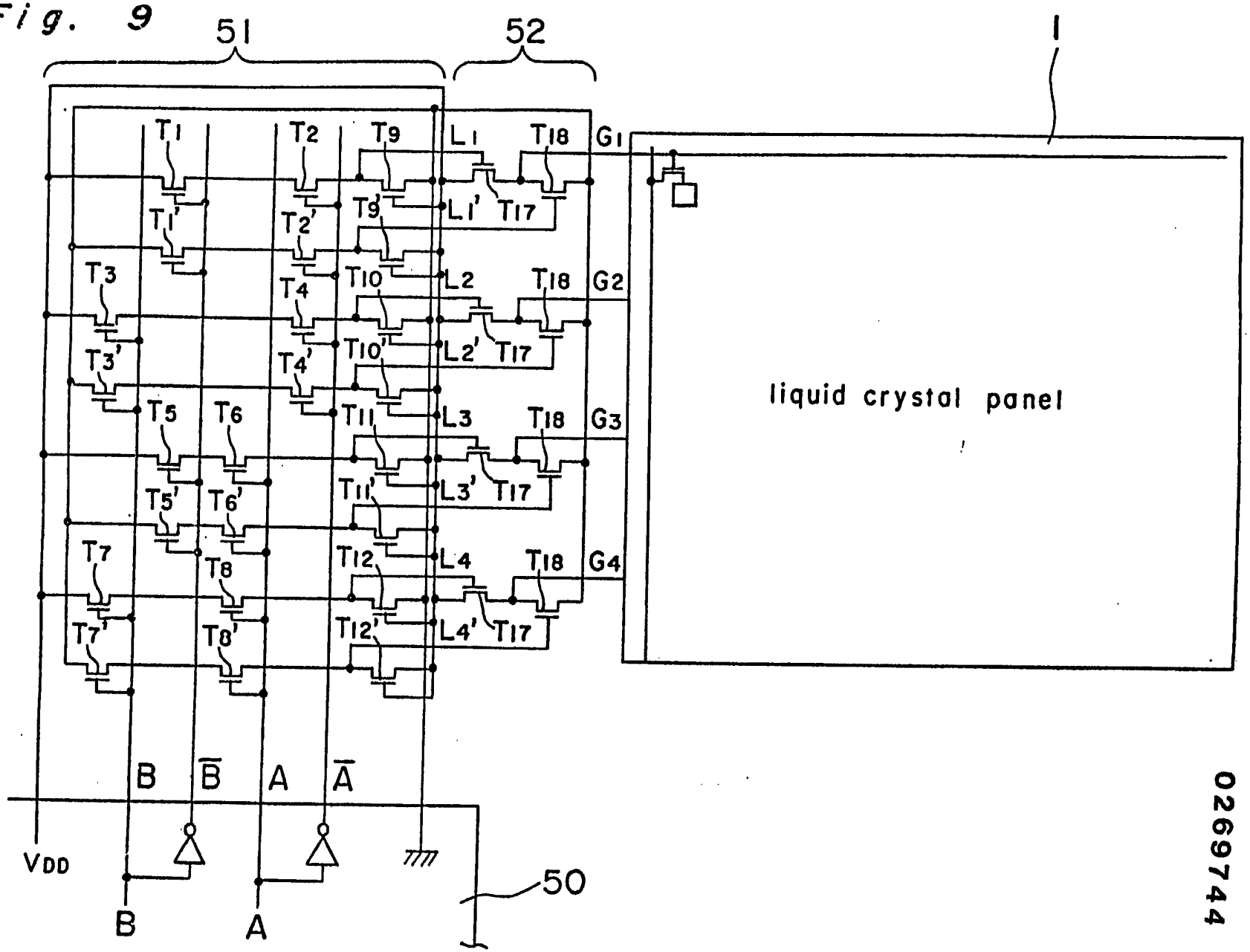

liquid crystal panel
1
output circuit
52
50
51
G1
G2
G3
G4
D1
D2
D3
D4
D5
D6
D7
D8
$\bar{A}$
A
$\bar{B}$
B
V_{DD}
T9
T10
T11
T12

Fig. 8

Fig. 9



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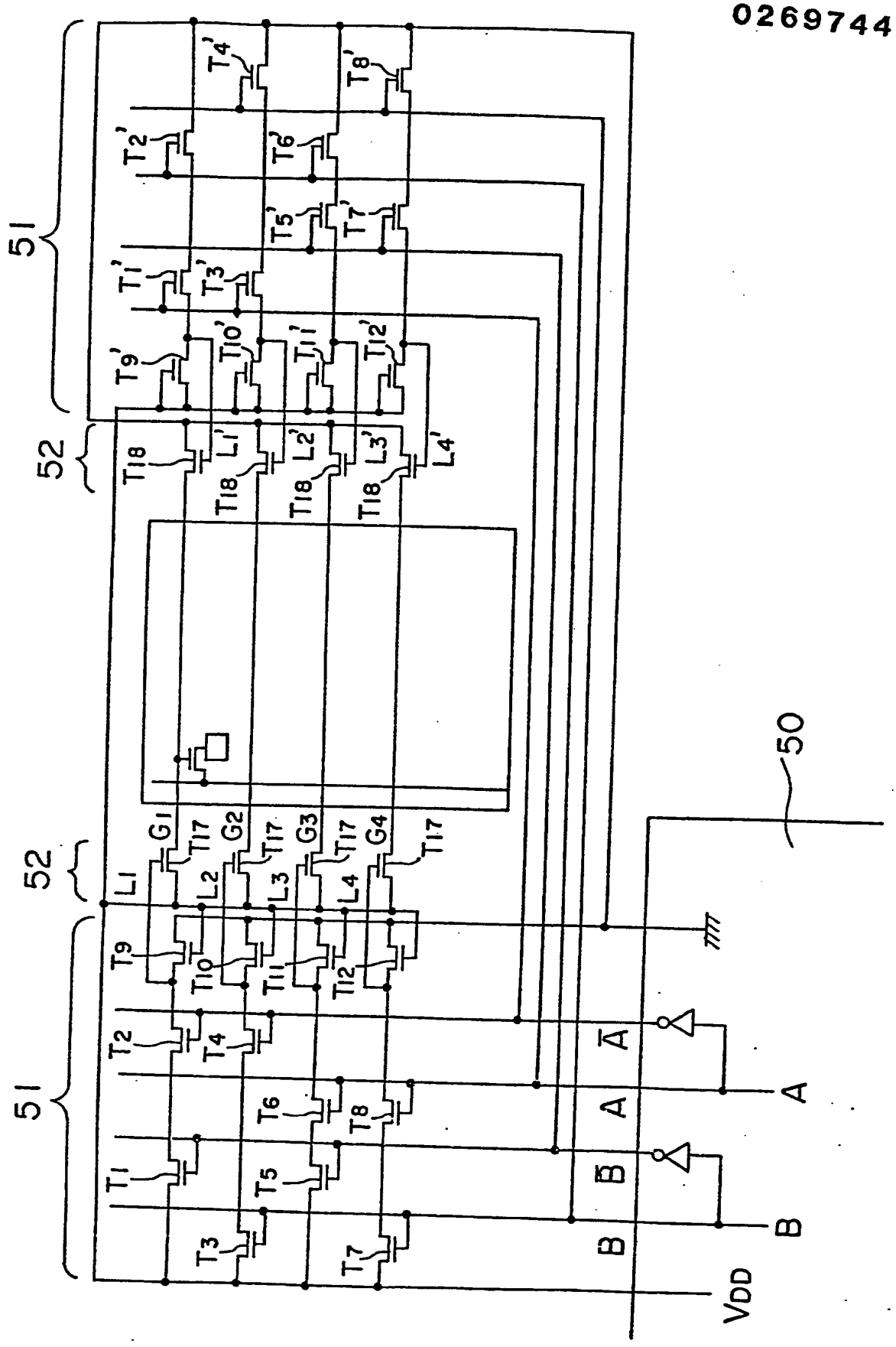

51
52
52
51
T1'
T2'
T3'
T4'
T5'
T6'
T7'
T8'
T9'
T10'
T11'
T12'
T18
L1'
L2'
L3'
L4'
G1
G2
G3
G4
T17
L1
L2
L3
L4
T9
T10
T11
T12
T2
T4
T6
T8
T1
T5
T3
T7
50
A
B
VDD

Fig. 10

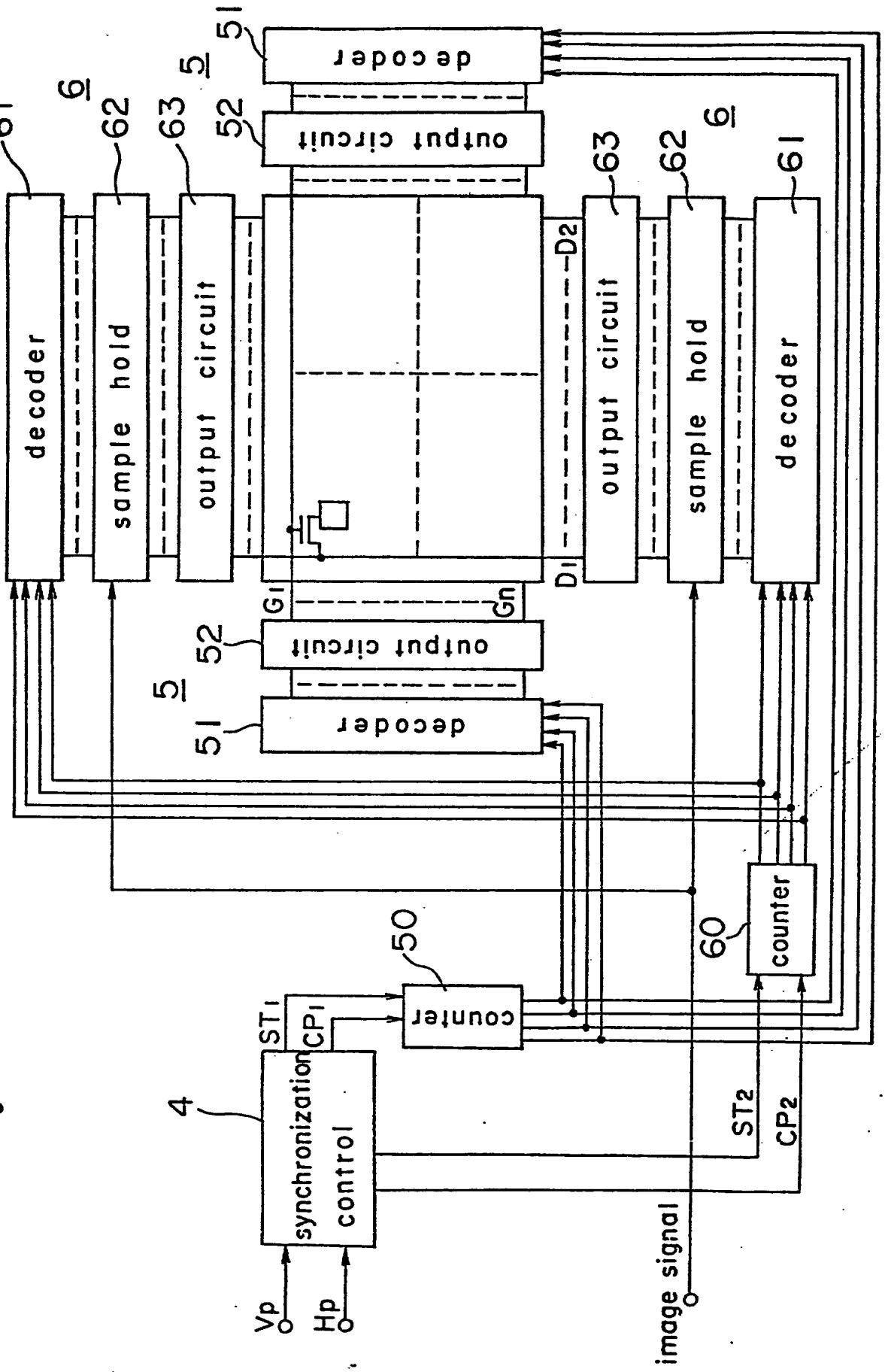

5
51
decoder
52
output circuit
6
61
62
63
decoder
sample hold
output circuit
D1
D2
G1
Gn
output circuit
sample hold
decoder
counter
60
50
counter
ST1
CP1
4
synchronization control
ST2
CP2
Vp
Hp
image signal

Fig. 11

0269744

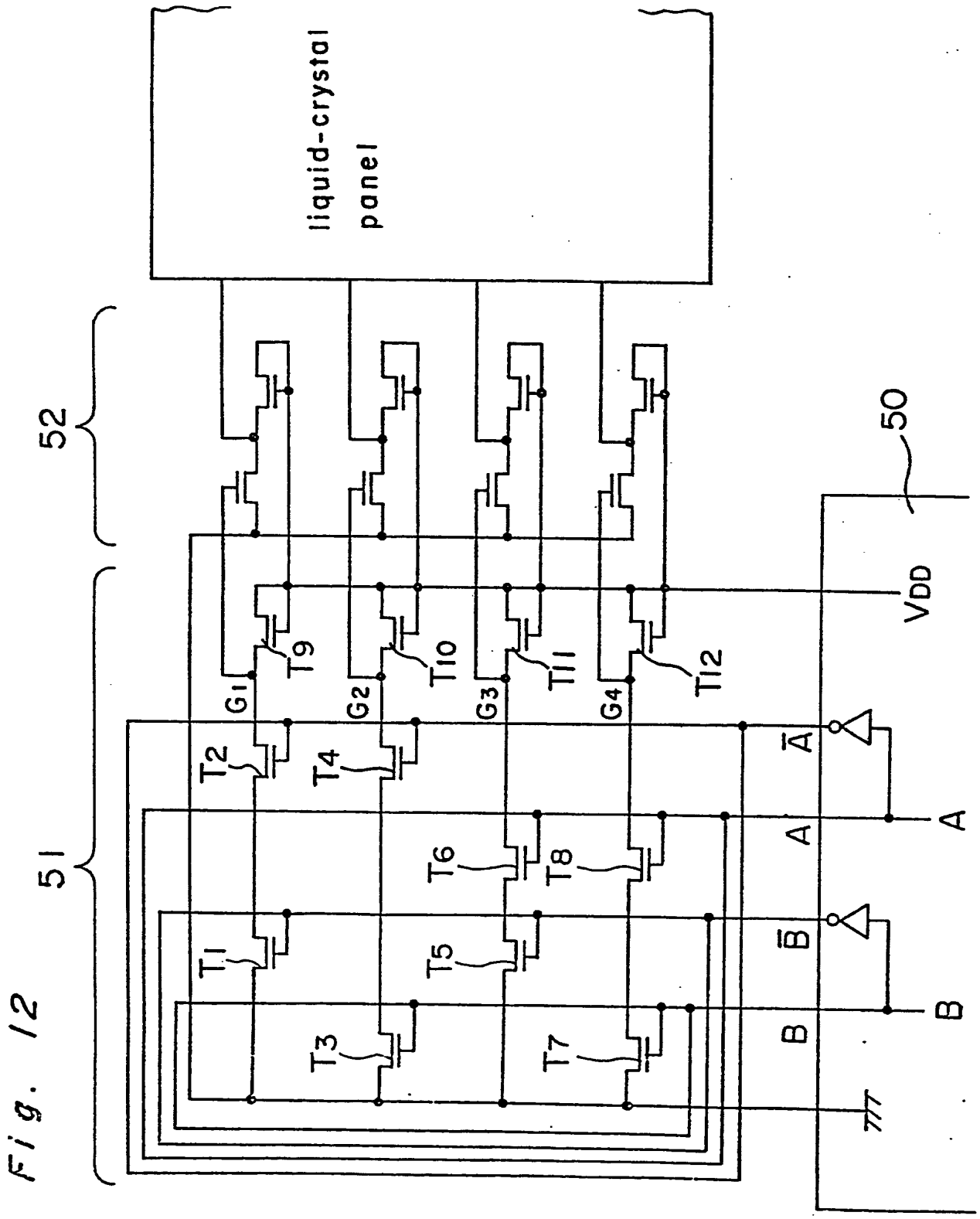


Fig. 12

Fig. 13

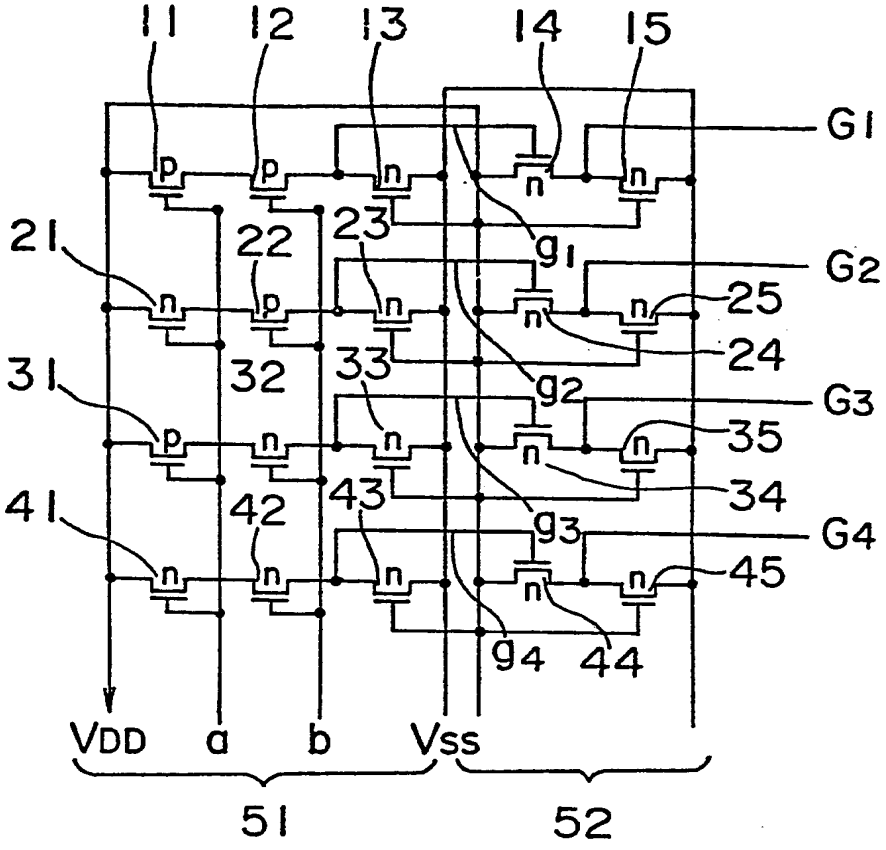

11
12
13
14
15
G1
21
22
23
g1
G2
25
24
31
32
33
g2
G3
35
34
41
42
43
g3
G4
45
g4
44
VDD
a
b
Vss
51
52

Fig. 14

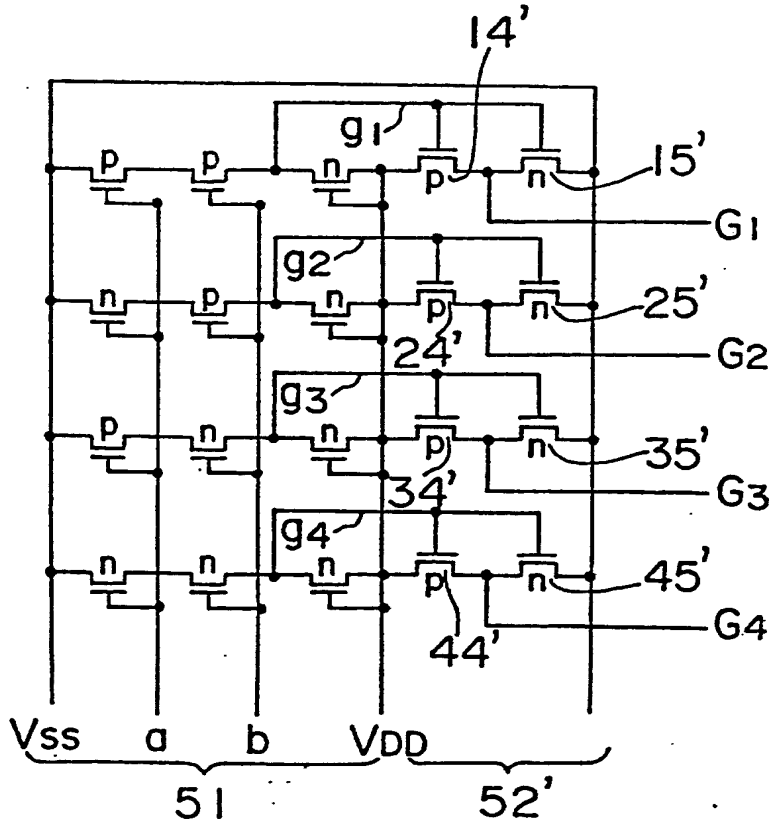

14'
g1
15'
G1
g2
25'
24'
G2
g3
35'
34'
G3
g4
45'
44'
G4
Vss
a
b
VDD
51
52'

Fig. 15

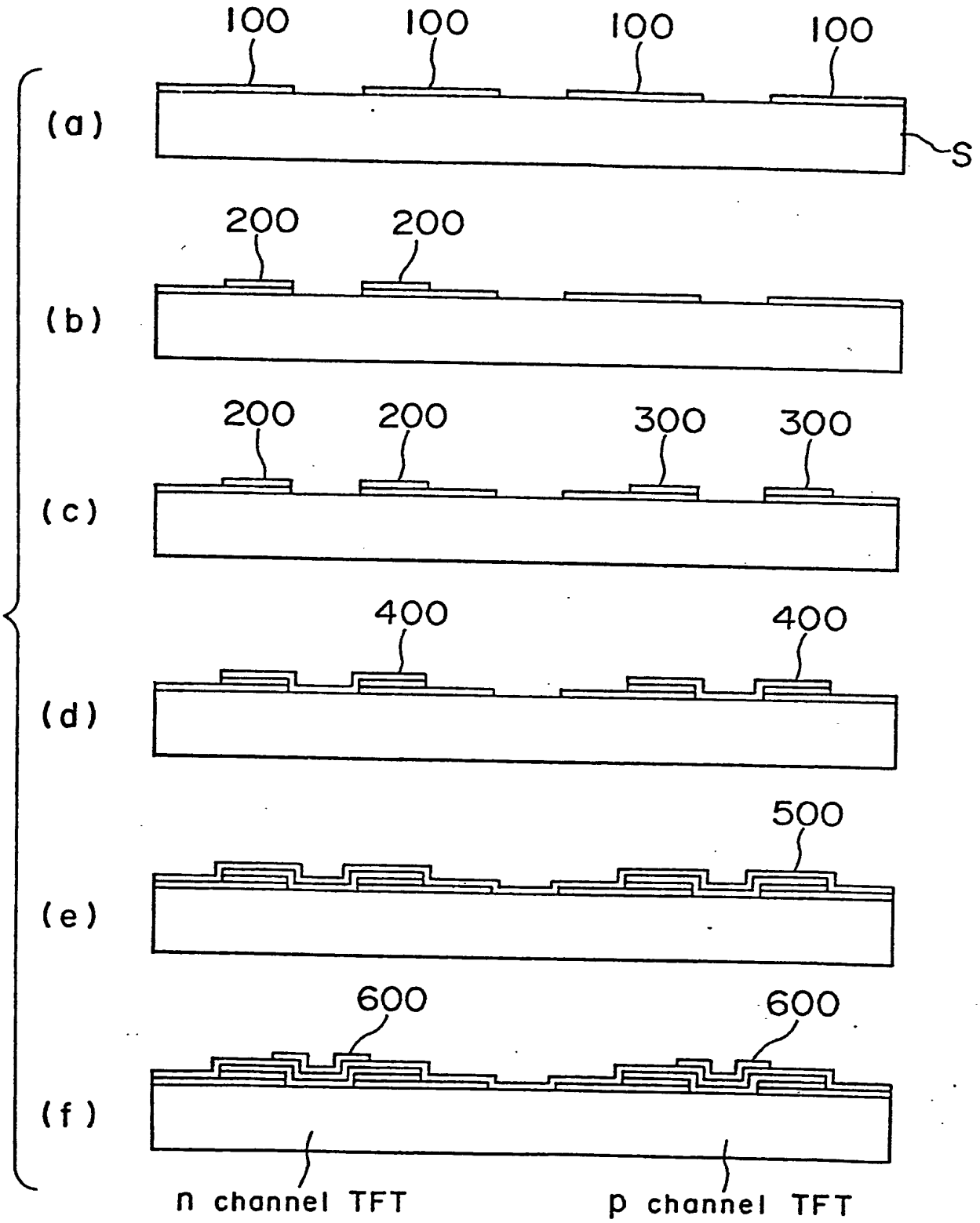

100
100
100
100
(a)
S
200
200
(b)
200
200
300
300
(c)
400
400
(d)
500
(e)
600
600
(f)
n channel TFT
p channel TFT

Fig. 16

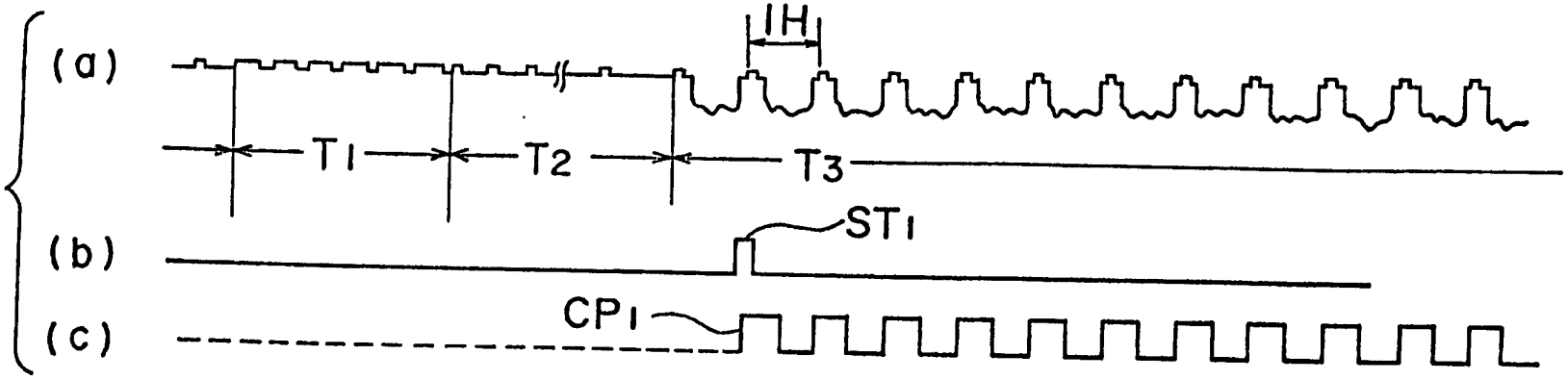
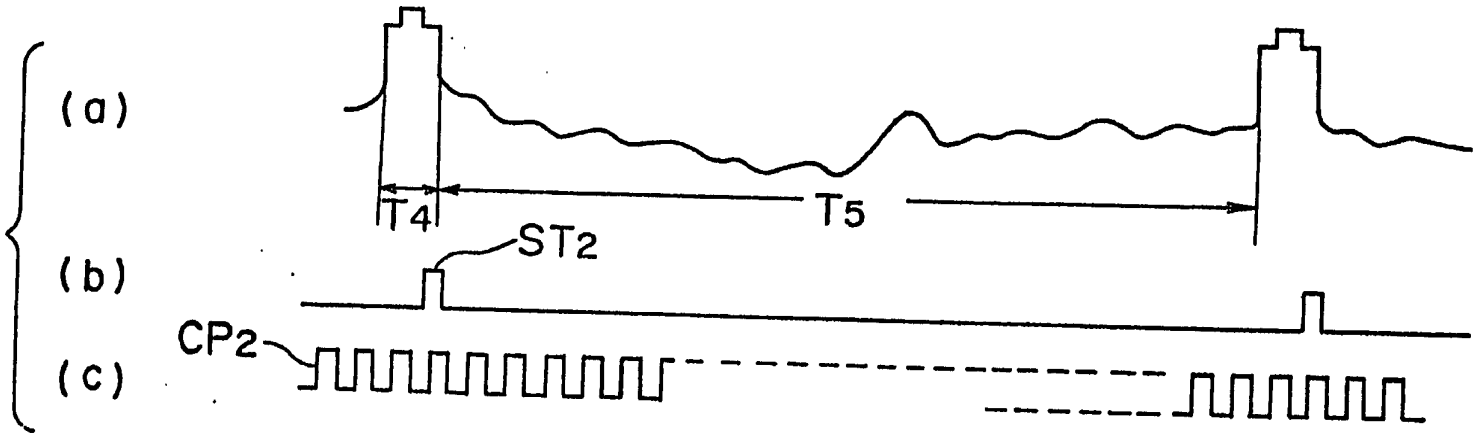


Fig. 17



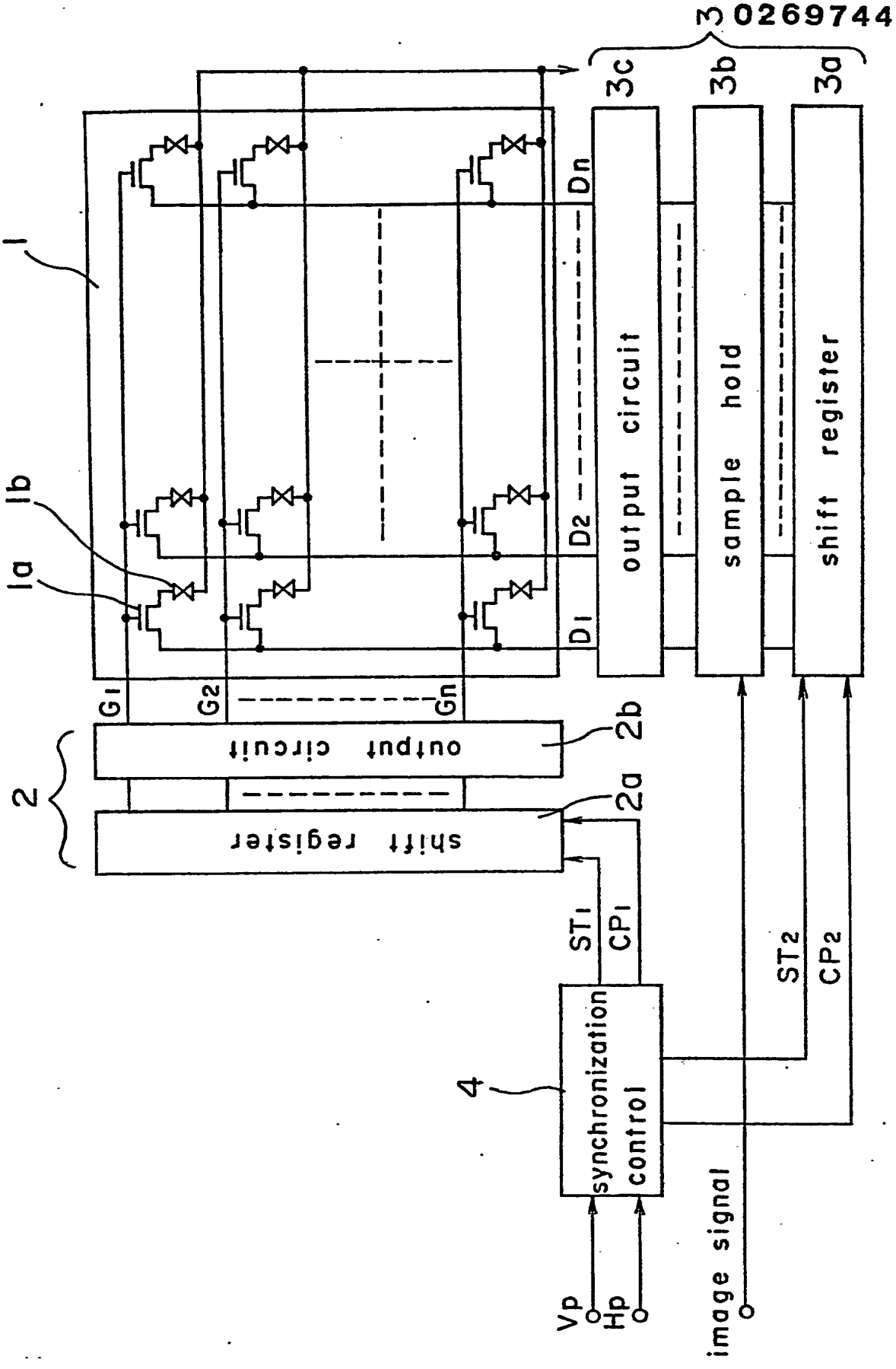

3
3c
3b
3a
output circuit
sample hold
shift register
1
1b
1a
Dn
D2
D1
G1
G2
Gn
2
output circuit
2b
shift register
2a
ST1
CP1
ST2
CP2
4
synchronization control
Vp
Hp
image signal

Fig. 18

0269744

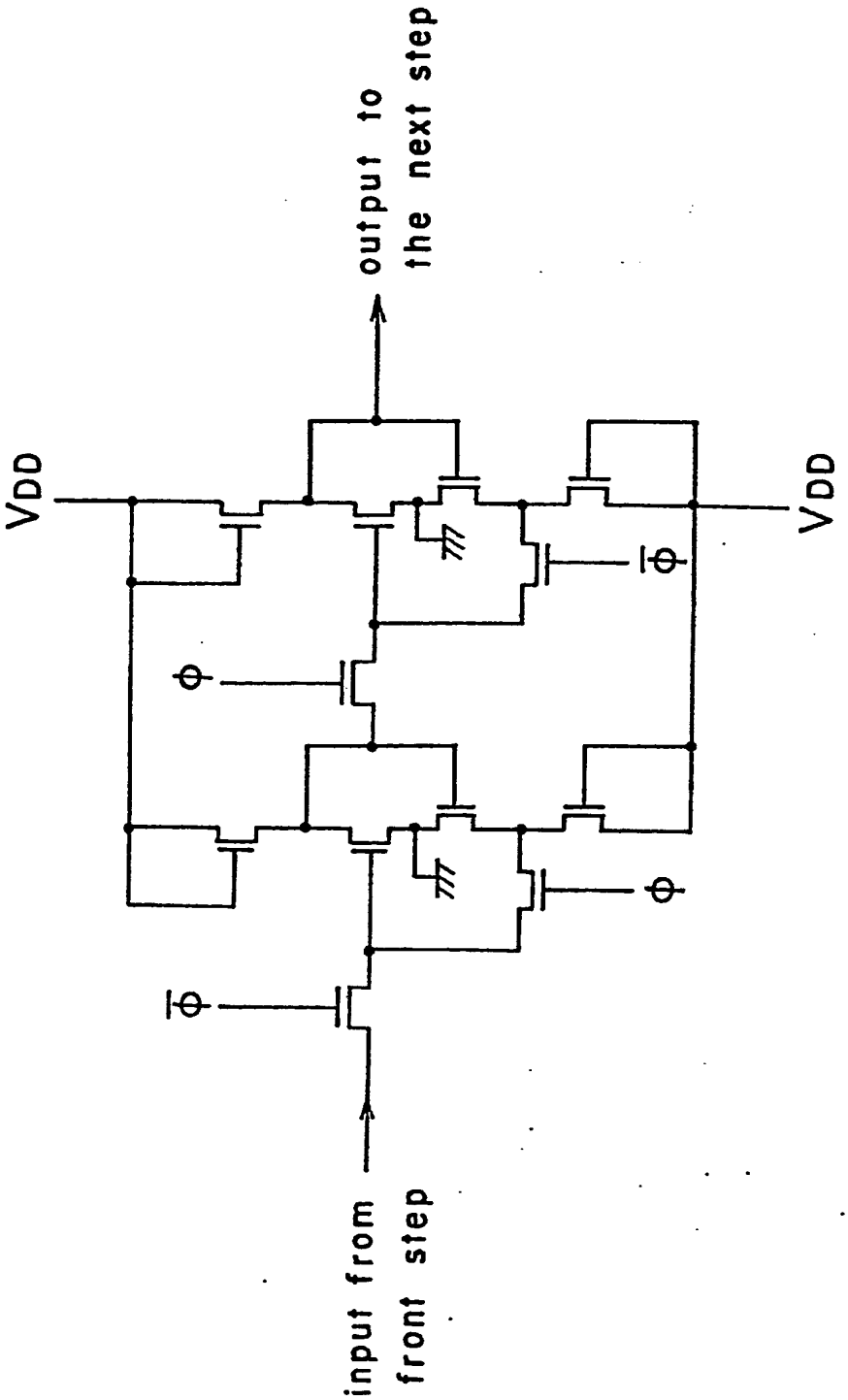


Fig. 19

INTERNATIONAL SEARCH REPORT

International Application No PCT/JP87/00294

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl[4] G09G3/36, G09G3/20

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC	G09G3/36, G09G3/20

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

Jitsuyo Shinan Koho 1926 - 1987
Kokai Jitsuyo Shinan Koho 1971 - 1987

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	JP, A, 56-87089 (Daini Seikosha Co., Ltd.) 15 July 1981 (15. 07. 81) Page 540, upper left column to upper right column, line 6, Fig. 3 (Family: none)	1
X	JP, A, 53-116742 (Westinghouse Electric Corp.) 12 October 1978 (12. 10. 78) Page 254, lower left column, lines 7 to 20 & US, A, 4,114,070 & GB, A, 1,573,879 & DE, A1, 2,810,470 & FR, A1, 2,385,164 & NL, A, 7,802,863	1
Y	JP, A, 56-87089 (Daini Seikosha Co., Ltd.) 15 July 1981 (15. 07. 81) Page 540, upper left column to upper right column, line 6, Fig. 3	2-10
Y	JP, A, 53-116742 (Westinghouse Electric Corp.)	2-10

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
August 3, 1987 (03. 08. 87)	August 17, 1987 (17. 08. 87)
International Searching Authority [1]	**Signature of Authorized Officer [20]**
Japanese Patent Office	

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

& US, A, 3,781,864 & GB, A, 1,371,990
& HK, A, 42,676

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE[10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers..... because they relate to subject matter[12] not required to be searched by this Authority, namely:

2. ☐ Claim numbers..... because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out[13], specifically:

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING[11]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

	12 October 1978 (12. 10. 78) Page 254, lower left column, lines 7 to 20, Fig. 4	
Y	JP, A, 54-154992 (Suwa Seikosha Kabushiki Kaisha) 6 December 1979 (06. 12. 79) Page 547, lower left column, lines 5 to 10 (Family: none)	2, 3
Y	JP, A, 47-22094 (Suwa Seikosha Kabushiki Kaisha) 6 October 1972 (06. 10. 72) Page 634, upper left column, line 14 to upper right column, line 16, Fig. 2	4-10

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers....., because they relate to subject matter [12] not required to be searched by this Authority, namely:

2. ☐ Claim numbers....., because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [11]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.